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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,870	06/27/2003	Mark T. Bohr	42P15335	7488

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/608,870	BOHR ET AL.
	Examiner	Art Unit
	Dao H. Nguyen	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-26* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-16, and 25-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination (RCE) filed 06/27/2005.

Claims 1-8, and 10-26 are active in this application.

Claim(s) 9 and 27 have been cancelled.

Remarks

2. Applicant's arguments filed on 06/27/2005 have been fully considered, but are moot in view of the new ground of rejections.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 1-8, 10, 14-16, and 25-26 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,121,100 to Andideh et al.

Regarding claim 1, Andideh discloses an apparatus, as shown in figs. 2-3, comprising:

a substrate 201;

a device including a gate electrode 204 on a surface 203 of the substrate 201 and a first and a second junction regions 211 in the substrate 201 adjacent the gate electrode 204; and

an epitaxial layer 217 comprising a silicon alloy material (col. 3, lines 5-40) disposed in each of the first and the second junction regions 211 such that a surface of the first junction region and a surface of the second junction region 211 are in a non-planar relationship with the surface 203 of the substrate 201, and the silicon alloy material 217 extends below the surface of the substrate 201. See fig. 2, and also col. 4, lines 13-34; col. 6, line 40 to col. 7, line 62; col. 9, lines 10-29.

Regarding claim 2, Andideh discloses the apparatus wherein a surface 203 of the substrate defines a top surface of the substrate and the surface of the first junction region and the surface of the second junction region are superior to the top surface of the substrate. See fig. 2, and col. 6, line 40 to col. 7, line39.

Regarding claim 3, Andideh discloses the apparatus wherein the surface of the first junction region and the surface of the second junction region are superior to the top

surface of the substrate by a length in the range of between 5 nanometers and 150 nanometers. See col. 6, lines 23-38, and lines 55-59.

Regarding claim 4, Andideh discloses the apparatus wherein the first junction region and the second junction region 211 define a depth in the range of between 30 nanometers and 250 nanometers in depth below the surface 203 of the substrate 201. See col. 6, lines 23-38, and lines 55-59.

Regarding claim 5, Andideh discloses the apparatus wherein the substrate is under a strain caused by a silicon alloy lattice spacing of the silicon alloy. This is inherent since a lower layer must always suffer a (compressive) strain caused by a layer atop it. See also figs. 3, and col. 7, line 40 to col. 8, line 51.

Regarding claim 6, Andideh discloses the apparatus wherein the silicon alloy material 217 has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material. This is inherent due to different materials and/or formations of the substrate and the silicon alloy. See col. 4, lines 13-34 and col. 7, lines 1-39.

Regarding claim 7, Andideh discloses the apparatus wherein the substrate is under a compressive strain caused by the silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material. See col. 4, lines 13-34, and col. 6, lines 59-65.

Regarding claim 8, Andideh discloses the apparatus wherein a surface 203 of the substrate 201 proximate to the first junction region 211 defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region 211 defines a second substrate sidewall surface and the silicon alloy material disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface (sidewall spacer 206). See figs. 2-3.

Regarding claim 10, Andideh discloses the apparatus wherein the silicon alloy material comprises one of silicon germanium, silicon carbide, nickel silicide, titanium silicide, and cobalt silicide. See col. 7, lines 13-39.

Regarding claim 14, Andideh discloses an apparatus, as shown in figs. 2-3, comprising:

a substrate 201;

a device including a gate electrode 204 on a top surface 203 of the substrate 201 and a first and a second junction regions 211 in the substrate adjacent the gate electrode 204; and

a silicon alloy material 217 (col. 3, lines 5-40) having a silicon alloy lattice spacing that is different

than a lattice spacing of the substrate 201 (this is inherent due to different materials and/or formations of the substrate and the silicon alloy; see col. 4, lines 13-34 and col. 7, lines 1-39) disposed in each of the first junction region and the second junction region 211 such that a surface of the first junction region 211 and a surface of the second junction region 211 are superior to the top surface of the substrate 201 by a length sufficient to cause a strain in the substrate, and the silicon alloy material 217 extends below the surface of the substrate 201. See fig. 2, and also col. 4, lines 13-34; col. 6, line 40 to col. 7, line 62; col. 9, lines 10-29.

Regarding claim 15, Andideh discloses the apparatus wherein the substrate 201 comprises an N-type channel/well material of one of silicon, polycrystalline silicon, and single crystal silicon having an electrically negative charge, and wherein the silicon alloy material comprises a P-type junction region material having an electrically positive charge. See col. 4, lines 13-34, and col. 6, line 40 to col. 7, line 39.

Regarding claim 16, Andideh discloses the apparatus wherein the silicon alloy is silicon germanium having a lattice spacing that is larger than a lattice spacing of the N-type channel/well material and wherein the strain is a compressive strain. See figs. 3, and col. 4, lines 13-34, and col. 6, line 40 to col. 7, line 39.

Regarding claim 25, Andideh discloses an apparatus, as shown in figs. 2-3, comprising:

a substrate 201;

a device including a gate electrode 204 on a surface 203 of the substrate and a first and a second junction regions 211 in the substrate 201 adjacent the gate electrode 204; and

an epitaxial layer comprising a silicon alloy material 217 disposed in each of the first and the second junction regions 211 such that a surface of the first junction region and a surface of the second junction region are in a non-planar relationship with the surface 203 of the substrate 201, wherein the silicon alloy material 217 has one of a same crystallographic characteristic, a same crystal structure and a same crystal grade as the substrate, and

the silicon alloy material 217 extends below the surface of the substrate 201. See fig. 2, and also col. 4, lines 13-34; col. 6, line 40 to col. 7, line 62; col. 9, lines 10-29.

Regarding claim 26, Andideh discloses the apparatus wherein the substrate is under a strain caused by the silicon alloy material having a lattice spacing that is different than a lattice spacing of the substrate. See col. 4, lines 13-34, and col. 6, lines 59-65.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim(s) 11-13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,121,100 to Andideh et al, in view of Kim, U.S. Patent No. 6,878,597, and further in view of the following remarks.

Regarding claim 11, Andideh discloses the apparatus further comprising a layer of silidde material 218 on the surface of the first junction region, the surface of the second junction region 211, and the gate electrode 204.

Andideh is silent about the material of the silicide layer.

However, Kim discloses an apparatus, as shown in figs. 5-7, and 13, comprising substrate 100, first and second source/drain junction regions 130, gate structure 115, and silicide layers 137 cover the source/drain regions 130 and the gate structure 115, wherein material of the silicide layer includes one of nickel silicide, titanium silicide, and cobalt silicide (col. 5, line 52 to col. 6, line 16).

It would have been obvious to one having ordinary skill in the art at the time the invention was made that the silicide layer of Andideh could also be made by materials as those of Kim, since it has been well known in the art that such materials are common

materials for a silicide layer. See further U.S. Patent No. 6,653,700 to Chau et al., col. 8, line 53 to col. 9, line 2.

Regarding claims 12 and 13, Andideh discloses the apparatus comprising all claimed limitations, except for a conformal etch stop material and a layer of dielectric material on top of the silicide layer.

Kim discloses an apparatus comprising a conformal etch stop material 140 on the silicide layer 137, wherein the conformal etch stop material comprises one of silicon dioxide, phosphosilicate glass, silicon nitride, and silicon carbide, and wherein the layer of dielectric material comprises one of carbon doped oxide, cubic boron nitride, silicon dioxide, phosphosilicate glass, silicon nitride, fluorinated silicate glass, and silicon carbide. See figs. 5-7 and 13, and col. 6, lines 27-44.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Andideh to further include a conformal etch layer, and a layer of dielectric material as that of Kim in order to easily form contact holes, and, subsequently, contacts, to the source/drain junction regions and the gate structure, to provide accesses, and protections to the device.

Conclusion

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 13, 2005